ECE 3110 Spring 2016 Project: Transmission Lines and LTSpice Modeling

1 Introduction

In this team project you will be investigating three electrical engineering circuit and system topics where transmission lines come into play. The first is high frequency/microwave amplifier design employing impedance matching circuits. The second is stepped impedance transmission line lowpass filters. The third is being aware of transmission line effects in test and measurement, particularly when using a simple *BNC tee*.

To *jump-start* your work a collection of LTspice circuit simulation files is provided. Additionally custom design tools are provided for matching circuits and filters. FYI these tools step around the Smith chart making use of analytical techniques. These tools take the form of custom GUI apps and/or a Jupyter notebook containing code and examples. A ZIP file package is provided on the course Web Site.

Honor Code: The project teams will be limited to at most three members. Teams are to work independent of one another. Bring questions about the project to me. I encourage you to work in teams of at least two. Since each team member receives the same project grade, a group of two should attempt to give each team member equal responsibility. The due date for the completed project will be on or before 12:00 pm, Friday, April 22, 2016. Note: The 22nd is two weeks before the end of the semester.

2 Introduction and Problem Area Details

The first two problem areas, narrowband amplifiers and stepped line filters are part of wireless communication system design [1], while the test and measurement topic, is to make you more aware of what can happen if you are not careful in the lab.

2.1 Narrowband Microwave Amplifiers

In electronic circuits you learn about three terminal devices such as bipolar junction transistors (BJT) and field-effect transistors (FET). An amplifier, which produces a greater AC output voltage that the input AC voltage can be built using the FET as shown in Figure 1. **Note**: Biasing the device will not be considered in this project. The focus here is on the AC steady-state circuit model and how impedance matching circuits make the device useful as an amplifier.

At high frequencies the circuit model becomes more complex as device capacitance comes into play. Parasitics due to packaging are also a concern. Figure 2 shows the high frequency model used for this project and Figure 3 shows a simple package parasitics model. At its core the model is a voltage controlled current source, with gain g_m known as the low frequency transconductance. In general the gate-to-drain capacitance $C_{gd} > 0$. Here we make the assumption that the device is approximately *unilateral*, meaning no feedback from output to input, since $C_{gd} = 0$.

For the time being we ignore the package model, which if included would augment each of the device terminals with the LC circuit of Figure 4.

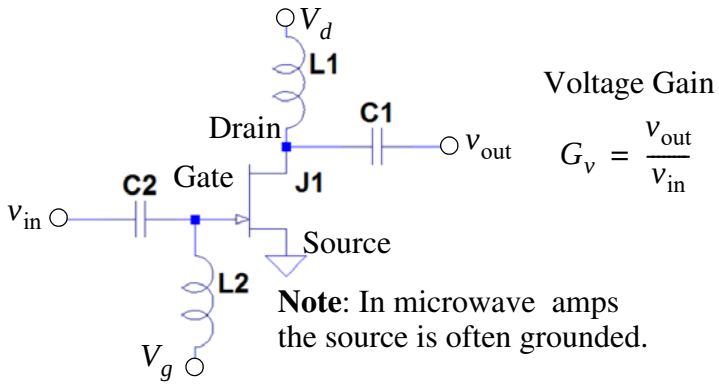

Figure 1: A simple *common source* amplifier.

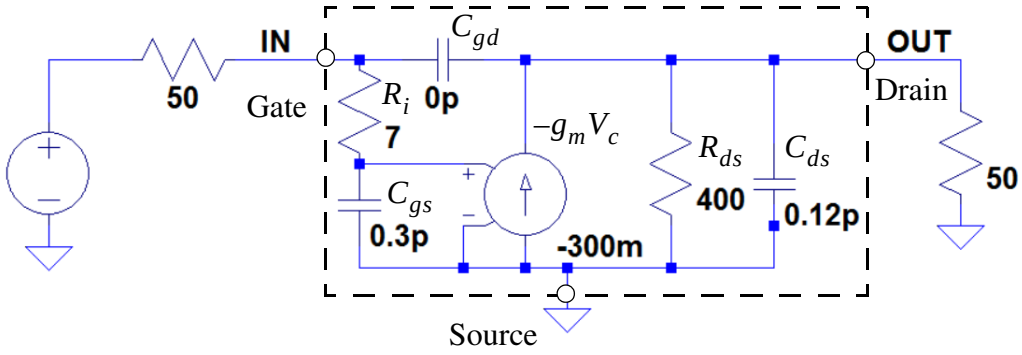

Figure 2: FET high frequency model with $C_{gd} = 0$ for unilateral considerations.

To make a microwave amplifier we embed the device model between two impedance matching circuits as shown in Figure 4.

2.1.1 Conjugate Matching for Maximum Gain

To achieve maximum gain in a Z_0 environment we choose $\Gamma_s = \Gamma_{\text{in}}^*$ and $\Gamma_L = \Gamma_{\text{out}}^*$ to achieve maximum power transfer. In general there are stability issues that must also be considered, but for this project we are ignoring these issues as the device has been made unconditionally stable by setting $C_{gd} = 0$. With $C\,gd > 0$ there is feedback from output to input and the two matching circuits interact with each other. The matching circuit design chosen here is a variation on the impedance matching circuits of text Chapter 2. Under conjugate matching and the unilateral assumption, the *maximum unilateral transducer gain*

$$G_{TU_{\max}} = \frac{1}{1-|\Gamma_{\text{in}}|^2} \cdot G_0 \cdot \frac{1}{1-|\Gamma_{\text{out}}|^2}$$

is achieved. Note G_0 is a function frequency and can be found from the device model.

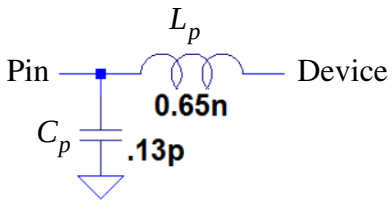

Figure 3: Series L-shunt C device package parasitics model.

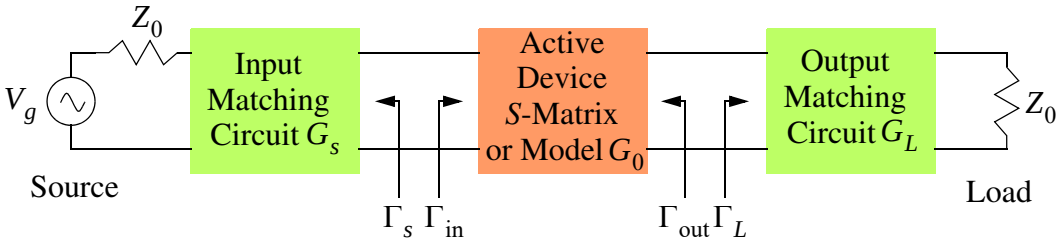

Figure 4: Narrow band amplifier design using input and output impedance matching circuits, where typically $\Gamma_s = \Gamma_{\text{in}}^*$ and $\Gamma_L = \Gamma_{\text{out}}^*$.

2.1.2 Matching Circuits

For this project the matching circuit topology is shown in Figure 5. The Smith chart can be used

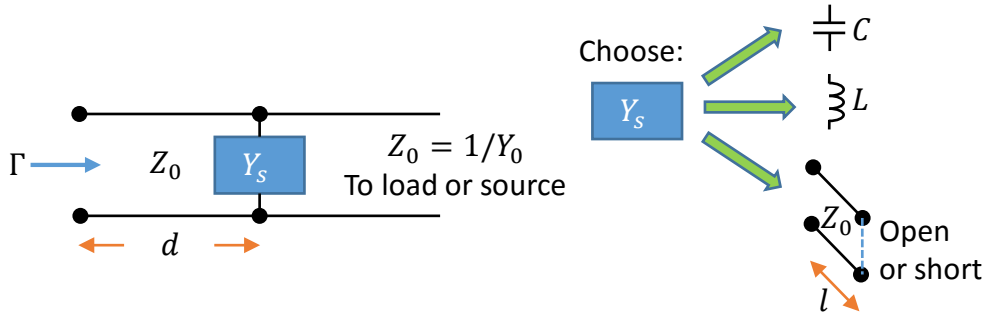

Figure 5: Common matching circuit design for a narrowband microwave amplifier.

to design this matching circuit, but analytical techniques work too. Here you will use a provided tool in either a Jupyter notebook (Python) or a stand-alone GUI as shown in Figure 6.

To drive the matching circuit designs you need to first measure Γ_{in} and Γ_{out}. An LTspice circuit can be configured to make these measurements using the technique of notes Chapter 2 p. 2–40. Here it was shown that given phasor voltage and current quantities at the measurement *plane* or interface from a Z_0 impedance source, we can obtain Γ as

$$\Gamma = \frac{V_{\text{tp}} - I_{\text{tp}} \cdot Z_0}{V_{\text{tp}} + I_{\text{tp}} \cdot Z_0}$$

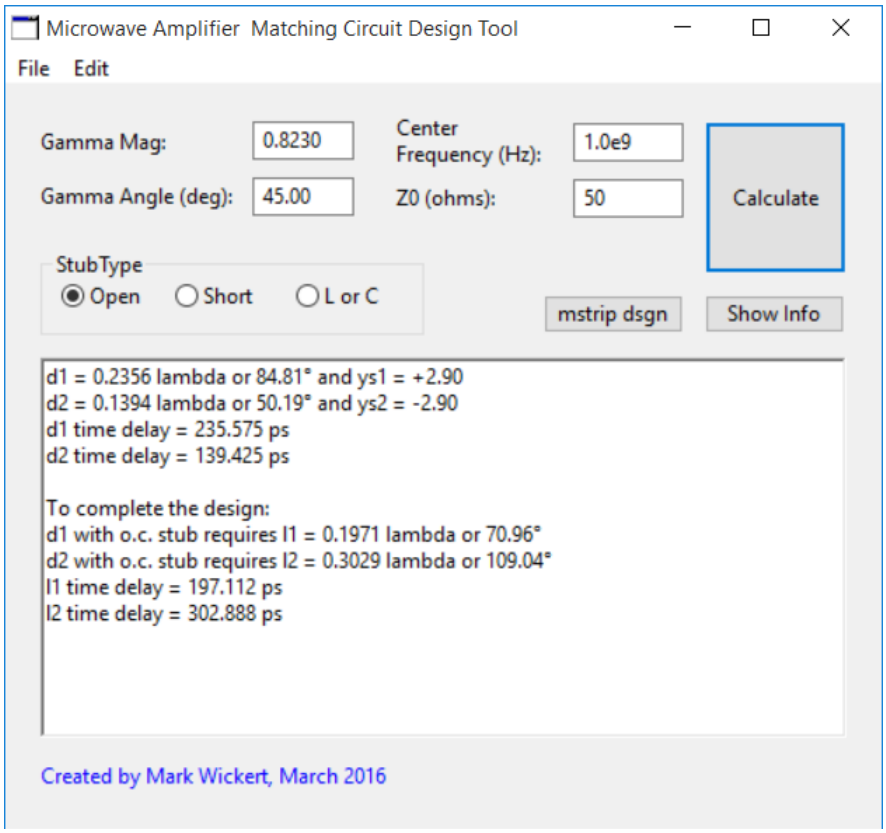

Figure 6: Matching circuit design using the tool `Amp_MatchingCkt_Design.exe`.

where here $Z_0 = 50$ and the subscript refers to the measurement test point, voltage and current are measured. Figure 7 shows how the above equation plays out in the amplifier design. Note Γ measurements taken in LTspice will have to be displayed using an equation with manual plot axes, in particular the magnitude should be set to display *Linear*, not the default *dB*. The magnitude and phase of Γ can then be read directly using the LTspice plot cursor tool. Since Γ is a function of frequency, you make your input/output measurements at the desired amplifier design center frequency.

In the project tasks you will design matching networks and implement them in an LTspice model similar to Figure 8. Here the conjugate input impedance matching networks were obtained with the aid of the GUI tool or Jupyter notebook. Note I have chosen short circuit shunt stubs, but other options are available. The design center frequency is at the global positioning system (GPS) L_1 carrier frequency of 1.57542 GHz. Perhaps the amplifier will be used as a preamp in a GPS receiver.

The design is verified by plotting the frequency response (see Figure 9) in dB by probing the `out` test point of Figure 8. This represents the true amplifier gain as the input AC voltage is $2\angle 0°$ and with just a Z_0 load and source resistor, the output is 1 V or 0 dB at all frequencies. As hoped for, the gain peaks at just over 31 dB at the design center frequency. Two additional measurements should be taken: (1) Measure the return loss at the input and (2) measure the return loss at the output. These measurements will confirm that conjugate matching to the device will also make

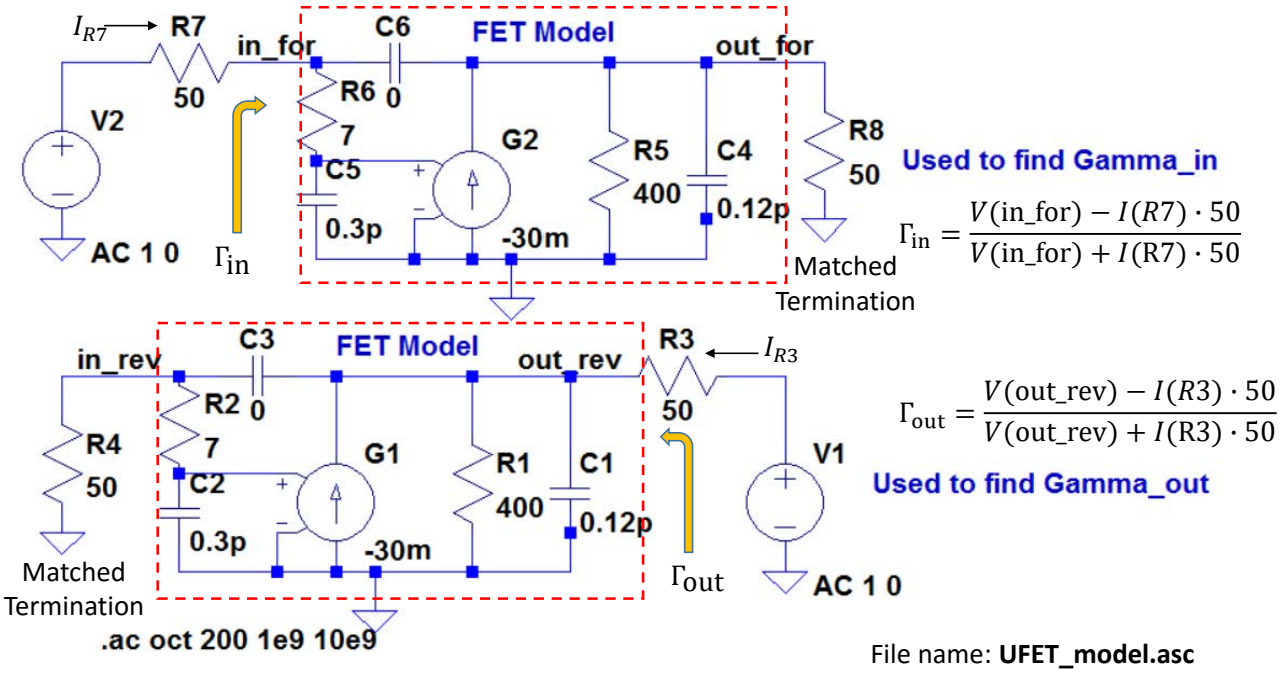

Figure 7: Test circuit for measuring Γ_{in} and Γ_{out}.

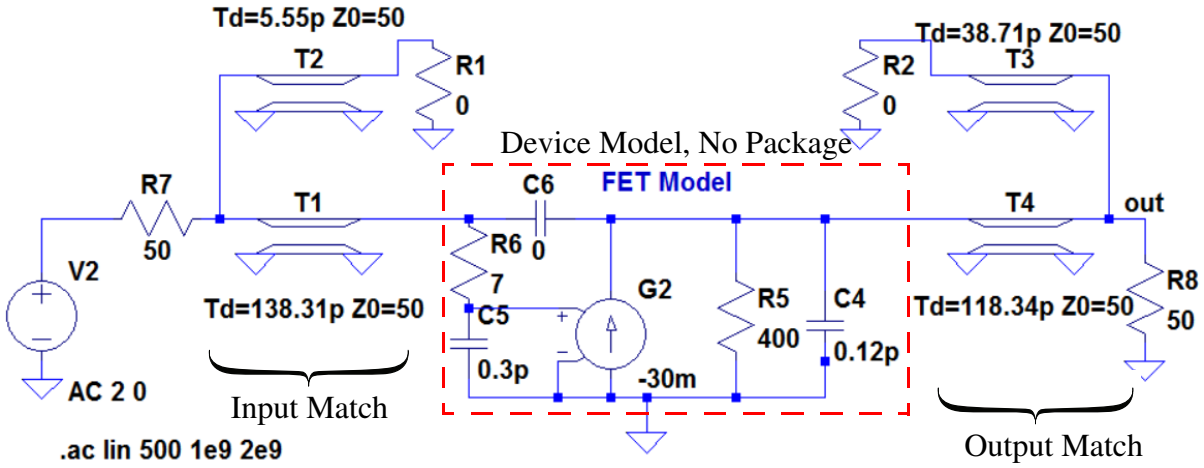

Figure 8: A sample amplifier design at 1.57542 GHz.

the input and out impedances of the amplifier match to the $Z_0 = 50$ source and load impedances. These two plots can be obtained using a test circuit similar to Figure 7, except now the input and output matching circuits need to be included. Recall that return loss is $-20\log_{10}(|\Gamma|)$.

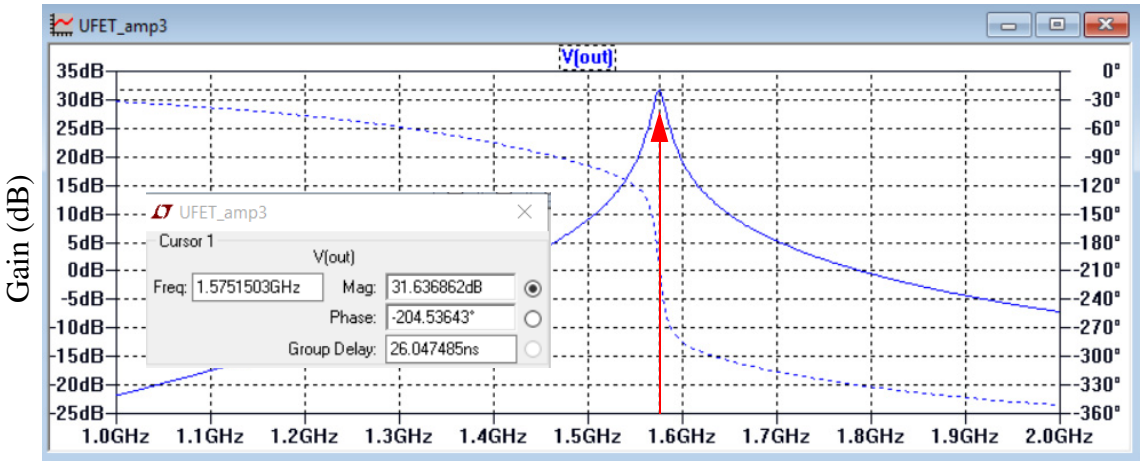

Figure 9: Sample amplifier design frequency response.

2.2 Stepped Line Lowpass Filters

Filter design is a topic that has received attention throught you signals and systems and circuits courses. Traditionally analog filters for microwave applications are designed using the *insertion loss* method [1], which yields the p*power loss ratio*

$$P_{\text{LR}} = \frac{\text{Power available from the source}}{\text{Power available from the load}} = \frac{P_{\text{inc}}}{P_{\text{load}}} = \frac{1}{1-|\Gamma(2\pi f)|^2},$$

where $\Gamma(2\pi f)$ is reflection coefficient seen looking into the filter when it is embedded in a properly source and load terminated environment. Popular P_{LR} characteristics are Butterworth (or maximally flat), which has a flat passband, and Chebyshev, which has equal ripple in the passband of the filter. The insertion loss design approach is summarized in Figure 10.

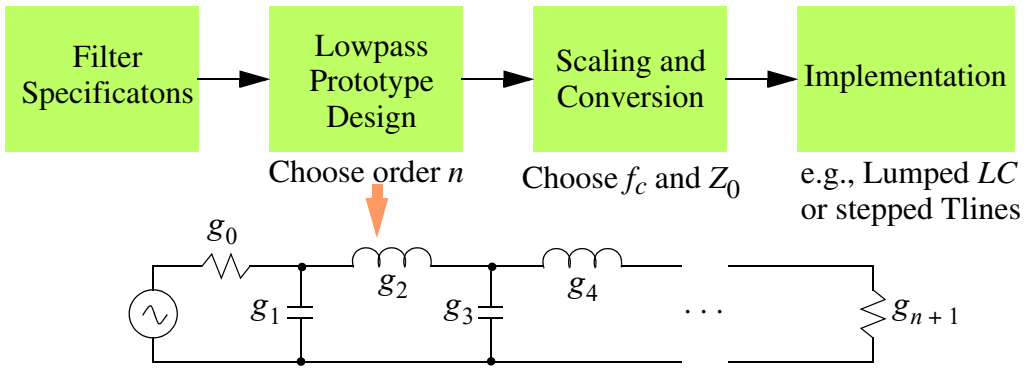

Figure 10: Insertion loss design process.

The filter specifications list gain or loss values at critical frequencies which lead to a lowpass filter prototype of a particular order, n. The operating impedance Z_0 and filter cutoff frequency, f_c, from the requirements and prototype together, move the design through scaling and

conversion, e.g., lumped element L and C values ready for implemention, or further conversion to yield another implementation form. In this project an alternative implementation form known as *stepped-impedance* filter design [1] is explored. At the top level the stepped-impedance approach is illustrated in Figure 11. The upper part of this figure shows the standard lumped element low-

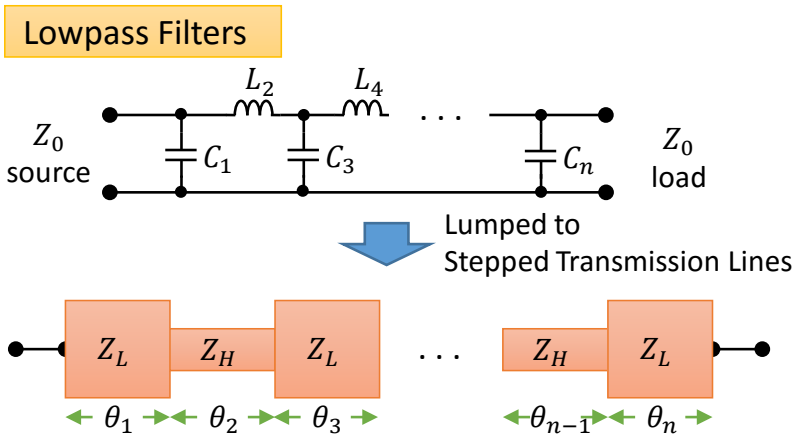

Figure 11: The stepped line lowpass filter compared with a standard lumped element LC filter.

pass using L's and C's. The stepped-impedance design, low portion of Figure 11) replaces each C with a short section of low characteristic impedance transmission line, Z_L, and each L with a short section of high characteristic impedance transmission line, Z_H. In microstrip transmission line, for example, the strip w/h value is very small (narrow width line) at high impedances and w/h is very large (wide line width) at low impedances. Intuitively a narrow line has high inductance per unit length (think L') and a wide line has large capacitance per unit length (think C'). Fabrication and higher-order electromagnetic effects limit both Z_H and Z_L. In this project we suggest Z_H of no more than 150 Ω and Z_L of no more than 10 Ω.

The design equations are based on the lumped element approximation to a short section of transmission line. From text Chapter 2A a differential section of line consists of a series inductor and a shunt capacitor. For a high impedance line the series inductive reactance dominates, so to synthesize an inductor we first note that

$$X_L \simeq Z_H \cdot \beta l$$

The required inductance via impedance scaling by Z_0 is

$$L = g_k \cdot Z_0$$

Putting the two equations together results in

$$\beta l_k = \theta_k = g_k \frac{Z_0}{Z_H} \text{ (rad)}$$

Note βl embodies f_c via the wavelength associated with the line electrical length. For a low impedance line the shunt capacitive susceptance dominates, thus

$$B_C \simeq \frac{1}{Z_L} \cdot \beta l$$

and the required capacitance via impedance scaling by Z_0 is

$$C = \frac{g_k}{Z_0}$$

Putting the two equations together results in

$$\beta l_k = \theta_k = g_k \frac{Z_L}{Z_0} \text{ (rad)}$$

In an LTspice model the line electrical lengths are replaced by their equivalent time delays at the desired cutoff frequency, f_c.

To allow easy exploration of the stepped-impedance approach a design tool is available in a Jupyter notebook or a custom GUI. Design requirements are kept simple by just providing the desired filter order, n and the cutoff frequency f_c in Hz. Additionally the user provides the ripple in dB for a Chebyshev design and the operating characteristic impedance. An $n = 5$ design is shown in Figure 12. The filter cutoff frequency is 2.0 GHz and ripple of the Chebyshev design is

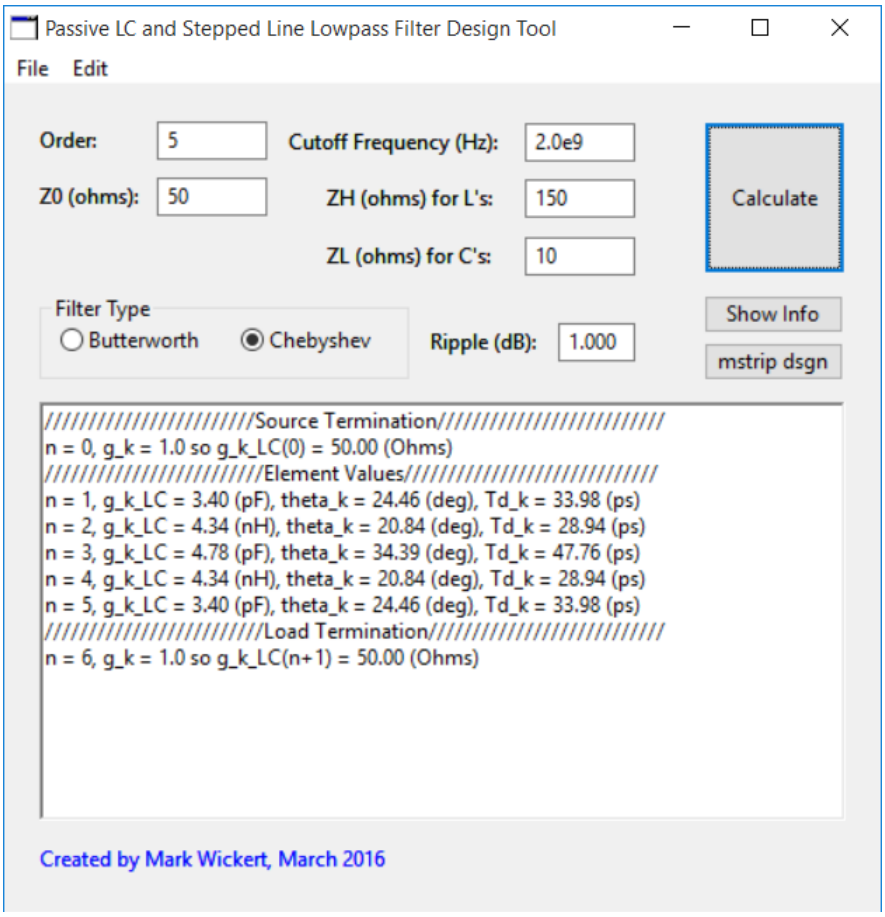

Figure 12: Stepped-impedance filter design tool `LC_Filter_Design.exe`.

left at the default value of 1 dB. Additionally $Z_H = 150\ \Omega$ and $Z_L = 10\ \Omega$. Fairly extreme values which you would see in a microstrip layout.

The design, as implemented in LTspice, is shown in Figure 13. What is not shown is a circuit layout in microstrip using polygons for the transmission line sections. The resulting frequency

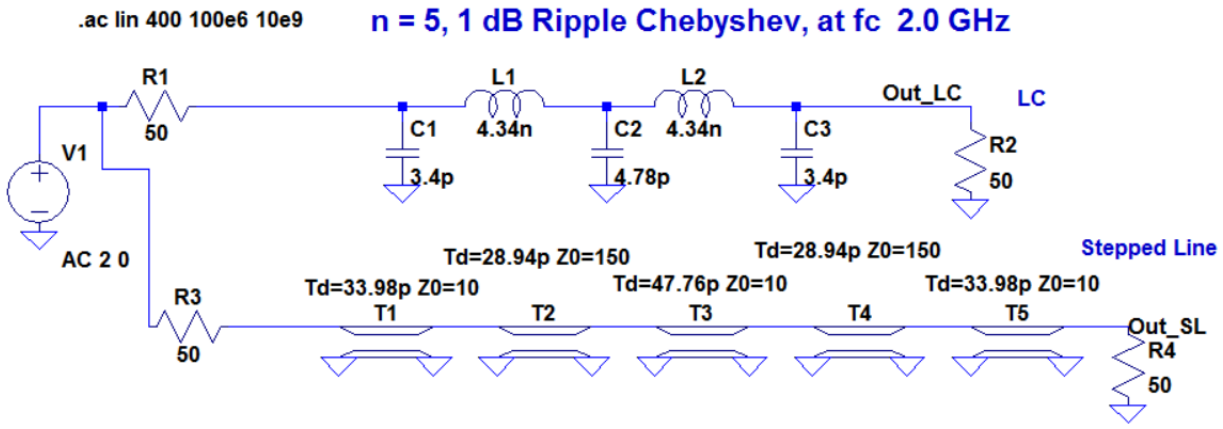

Figure 13: An LTspice $n = 5$ stepped-impedance Chebyshev design at 2.0 GHz.

response, comparing the stepped design to the true LC lumped designed is shown in Figure 14. You can see that the stepped-impedance design is close to the lumped filter, but not exact by any means. Why? Since the line lengths are essential exact, the lines are lossless, and there are no layout parasitics, we have to conclude the differences are due to distributed L and C values. If Z_H is decreased and/or Z_L is increased we expect the response differed to grow. The Z_H lines are adding unwanted shunt capacitance and the Z_L lines are adding unwanted series inductance. A microstrip implementation will also have to deal with parasitics due to the sudden change in line width as Z_H and Z_L sections are connected end-to-end. In the microwave circuits design world

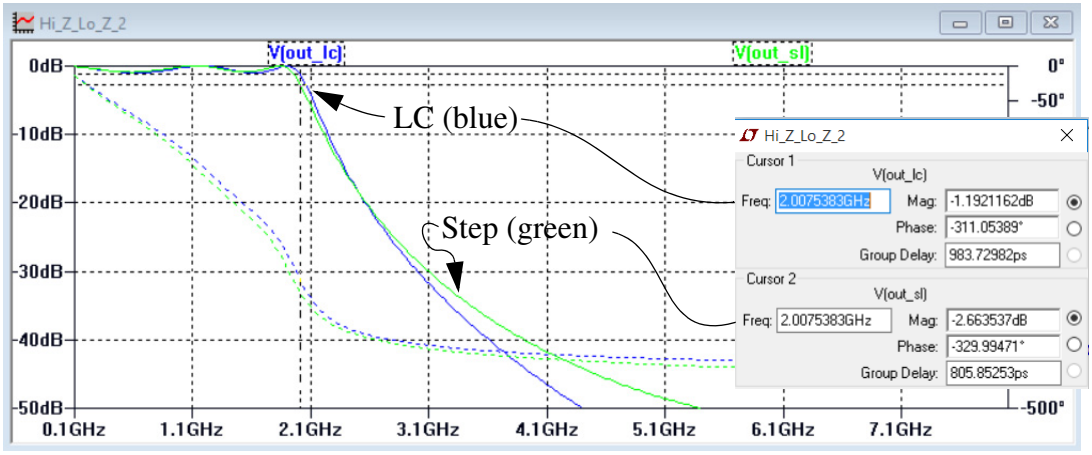

Figure 14: The 2.0 GHz filter frequency response, both LC and stepped designs.

microstrip discontinuity models are available or you may choose to perform a 2D or 3D EM field simulation of the actual layout using Ansoft HFSS [3] or Keysight EMPro [4], both of which we have available at UCCS.

2.3 Unexpected Transmission Line Issues in the Lab

This last topic is less rigorous than the first two. This part of the project focuses on what happens when you take measurements without thinking about transmission line effects. A classical example is how you might use a BNC tee to connect two instruments into the circuit at once. This arises when you say have a spectrum analyzer and an oscilloscope both available on the lab bench. The scope is your *eyes* into the time domain and the spectrum analyzer is your *eyes* into the frequency domain. The spectrum analyzer typically has a 50 Ω input impedance, while the scope is set to make high impedance (> 1 MΩ) measurements. Interfacing coax used in the lab is typically RG58, which has $Z_0 = 50$ Ω with a propagation velocity corresponding to about 8.5 inches/ns.

An LTspice model of one of many possible measurement scenarios is shown in Figure 15. At the top of the figure you see a reference circuit with a perfect measurement interface at 50 Ω, so no problems. The lower part of the figure shows an interface where two instruments are connected.

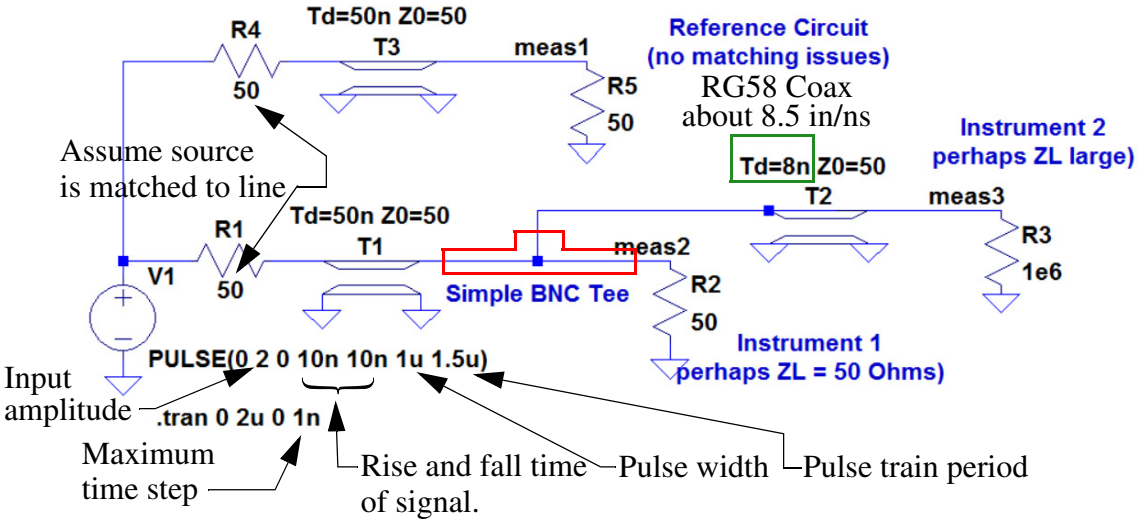

Figure 15: Making lab measurements and being aware of transmission line issues.

It might also be one instrument and one device under test. One load is *Instrument 1* is properly terminating the line. The BNC is tapping off and connecting a high impedance load *Instrument 2* via an 8ns cable (around 6ft as $8 \times 8.5 = 68$in). The waveforms that result from the exact LTspice settings of Figure 15 are shown in Figure 16. What jumps off the page is the ugly *ringing* at both the `meas2` and `meas3` test points. Can you explain what is happening?

3 Project Tasks

1. **Narrowband Microwave Amplifier Design**:

   (a) Design a narrow band amplifier at 5 GHz using the UFET model of Figure 2. The design should follow the general input/output matching circuit approach of Figure 4, with the various topology options of Figure 5. To obtain values for Γ_{in} and Γ_{out} use the provided LTspice schematic file `UFET_model.asc`, shown in Figure 7. You are free to

Figure 16: The three waveforms from the measurement scenario of Figure15.

choose any circuit topology you wish, as long as it taken from the designs provided by the GUI tool/Jupyter notebook. My preference is the stub-based designs. I also suggest you choose solutions that require the minimum line lengths for both the series and shunt lines. Implement your design using the LTspice reference schematic found in `UFET_amp_sample.asc` and shown in Figure 8.

(b) Test your design by obtaining a frequency response plot similar to the example design results of Figure 9. Note the peak gain and the amplifier 3 dB bandwidth relative to the peak gain.

(c) Plot the input and output return loss of the completed amplifier with matching circuits present (OK to plot the negative of this quantity as this is a little easier to do in LTspice). **Note**: To measure the output return loss you will need to move the AC generator from the input to the output.

(d) *Package Parasitics* (on hold for now) – Rework the amplifier design with the package parasitics model added to all three terminals of the device. This will require a new measurement of Γ_{in} and Γ_{out}, as the device is now being viewed at the package terminals. Compare the amplifier gain frequency response only, to the original 5 GHz design. What is the performance penalty?

(e) *Microstrip Layout on CF-PTFE* (on hold for now) – To get a feel for the size of the amplifier, lay it out using a PowerPoint slide as your layout drawing tool. Assume a substrate height of $h = 1.5$ mm and $\epsilon_r = 11.2$. Note in power point you can set the height and width of a rectangle in inches using the menu Drawing Tools Format and noting the selectors at the far right of the toolbar. I suggest starting with 2:1 (i.e., 2 inches layout is 1 inch actual size) scaling if this is too small consider 4:1. In your layout provide a 500 mil 50 Ω feedline section at the terminals of the amplifier.

The microstrip design equations from the text and implemented in the Chapter 2 Jupyter notebook, are available in the GUI amplifier matching circuit design tool by clicking

the button mstrip dsgn. To move the layout process along I have also provided the PowerPoint file `Amplifier_Layout_template.ppt`. A top view of an SOT23 (SOT = small outline transistor) package is also included to place at the center of the layout. Ignore biasing, but do make note of the need for ground connections at the ends of short-circuit stubs (if used) and the grounded source of the device.

2. **Stepped-Impedance Microstrip Lowpass Filters**:

   (a) Design a 7th-order Chebyshev lowpass filter to have $f_c = 3.0$ GHz. Set the ripple to 0.5 dB. Then build a simulation model in LTspice. Use the sample schematic file `Stepped_Tline_sample.asc` (LTspice schematic file) as your starting point. For comparison purposes also build the lumped element LC design. Assume that $Z_H = 150\ \Omega$ and $Z_L = 10\ \Omega$.

   (b) Plot the filter gain from 100 MHz to 10 GHz. Scale the file gain axis to run from -50 to 0 dB (manually scalling in LTspice). You may notice that the response comes back up again at some point. The periodic impedance behavior of transmission lines, not found in lumped element circuits (ignoring parasitics of course) is responsible for this behavior.

   (c) *Microstrip Layout on FR4* – To get a feel for the size of the filter, lay the filter out using a PowerPoint slide as your layout drawing tool. You will be placing simple rectangular polygons end-to-end. Assume a substrate height of $h = 62.5$ mils and $\epsilon_r = 4.6$. Note in power point you can set the height and width of a rectangle in inches using the menu Drawing Tools Format and noting the selectors at the far right of the toolbar. I suggest starting with 1:1 scaling if this is too small consider 2:1 (i.e., 2 inches layout is 1 inch actual size). In your layout provide a 500 mil 50 Ω feedline section at each end of the filter.

   The microstrip design equations from the text and implemented in the Chapter 2 Jupyter notebook, are available in the GUI filter design tool by clicking the button mstrip dsgn as shown in Figure 17. To move the layout process along I have also provided the PowerPoint file `Filter_Layout_template.ppt`. A top view of an SMA connector is also included to place at each of the filter layout.

3. **Transmission Line Effects in Lab Measurements**: In this task you will do some experiments with the LTspice schematic `Tline_Tee.asc` shown in Figure 15. You will be making some changes to schematic, observe the measurement waveforms and draw conclusions. Measurement outcomes are influenced by the rise and fall time of the input pulse signal, which controls the *edge speed* of the pulse. If you right click over the source the dialog box shown in Figure 18 should appear. From this dialog it is easy to make changes to the source waveform.

   (a) Working in the schematic `Tline_Tee.asc` change the rise and fall time of the input waveform from 10 ns to 1 ns. Also change the delay time of the transmission line `T2` from 8 ns to 20 ns. Run the simulation and plot the waveforms at measurement points 1, 2, and 3. Zoom the plot into the rising edge activity that starts at 50 ns and continues on to say 180 ns. From your knowledge of transients on transmission lines explain

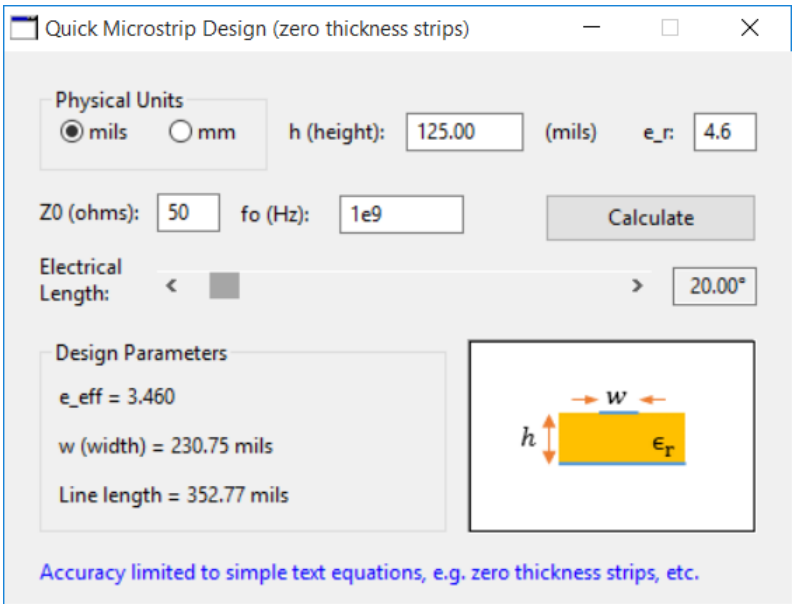

Figure 17: The microstrip design tool available inside the stepped-impedance filter design tool.

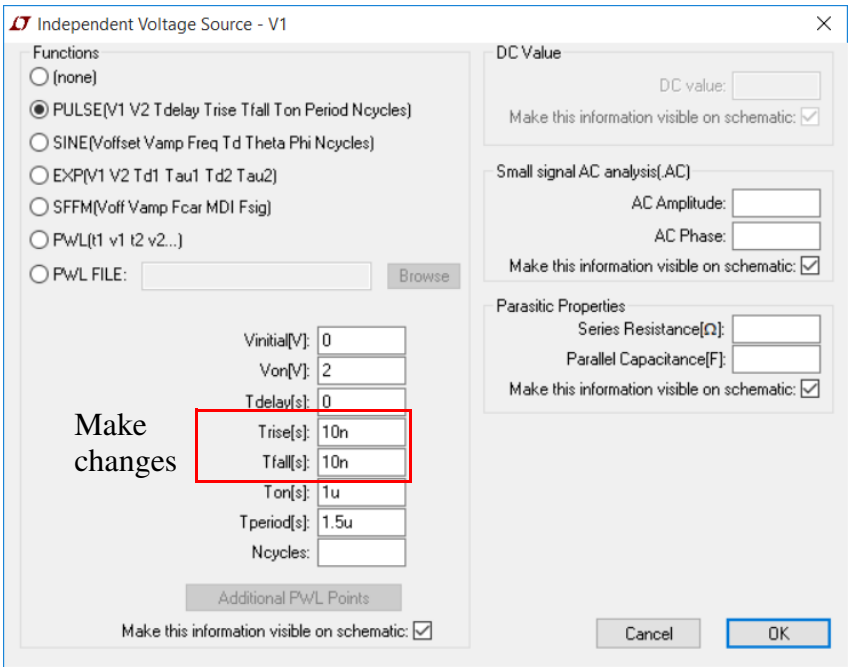

Figure 18: Settings available for an LTspice voltage source.

what you see. Especially focus on the `meas2` waveform. Include the plot in your report so you have something to talk from. A couple of sentences should do it.

(b) Repeat part (a) except now take the edge speed back to 10 ns and shorten the `T2` transmission line to just 2 ns ($\sim$ 17 inches of coax). Explain what you see. Do these results

make sense? Again include the plot in your report.

(c) Return the rise and fall times to 10 ns and set the length of `T2` back to 20 ns. Now set the load of `R2` to approximate an open circuit by making $R_2 = 1$ MΩ. Observe the waveforms. You should see the open circuit source voltage of 2 V. Why? The ringing is gone! Conveniently now the matched source impedance is absorbing all of the reflections. The generator voltage is now out of calibration relative to a 50 Ω load it is expecting to see.

Many more scenarios can be investigated. You hopefully have gained some additional understanding about test and measurement.

4. Summarize your experiences with this team project.

References

[1] David M. Pozar, *Microwave and RF Design of Wireless Systems*, John Wiley, 2001.

[2] F awwaz T. Ulaby and Umberto Ravaioli, *Fundamentals of Applied Electromagnetics*, seventh edition, Prentice Hall, New Jersey, 2015.

[3] http://ansys.com/Products/Electronics/ANSYS-HFSS.

[4] http://www.keysight.com/en/pc-1297143/empro-3d-em-simulation-software?cc=US&lc=eng